REMARKS

This amendment is being made pursuant to 37 C.F.R. §1.312. Accordingly, all pending claims in the instant application are allowed. Applicants have amended claims 180, 183, 187, 188, 190, and 191 to improve the form of these claims by providing proper antecedent basis. No new matter has been added. Applicant's respectfully request entry of the foregoing amendment.

Respectfully submitted,

Date: April 6, 2001

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Version With Markings to Show Changes Made

180. (amended) An integrated circuit device comprising:

input receiver circuitry to sample an operation code synchronously with respect to a first transition of an [the] external clock signal;

output driver circuitry to output data in response to the operation code specifying a read operation, wherein:

the output driver circuitry outputs a first portion of data in response to a rising edge transition of the [first] external clock signal; and

the output driver circuitry outputs a second portion of data in response to a falling edge transition of the [first] external clock signal.

183. (amended) The integrated circuit device of claim 182 wherein the input receiver [circuit] circuitry samples the address information synchronously with respect to a second transition of the external clock signal.

187. (amended) The integrated circuit device of claim 180 wherein both the rising and falling edge transitions of the [first] external clock signal include voltage swings of less than one volt.

188. (amended) The integrated circuit device of claim 180 wherein the rising edge transition of the [first] external clock

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signal and the falling edge transition of the external clock signal transpire in one clock cycle of the [first] external clock signal.

190. (amended) The integrated circuit device of claim 180 wherein the input receiver circuitry receives a value which is representative of a number of clock cycles of the external clock signal to transpire before the output [drivers] driver circuitry outputs data.

191. (amended) The integrated circuit device of claim 190 further including a programmable register to store the value which is representative of a number of clock cycles of the external clock signal to transpire before the output driver circuitry outputs data.

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